

Serial No. 09/546,833**PATENT**
Docket No. RAL920000042US1**Amendments to the Claims:**

1 - 3. (Canceled)

4. (Previously Presented) In a network switching system having an ingress processor for receiving incoming frames from a port of a network, and an egress processor having a port through which said frames are delivered, a method for enhancing processor speed comprising:

forming at said ingress processor a header for each frame destined for said egress processor having data for identifying a beginning of a processing sequence for said egress processor; and

decoding said data in said header in a hardware frame classifier into a starting address for said egress processor wherein decoding said data include indexing an address table in said hardware frame classifier; and executing processing from a starting address space identified by said table of said hardware classifier if said hardware classifier is enabled and executing processing of said frame beginning at a process execution level determined from a port configuration entry of the interface of the port said frame was received if a configuration bit of said egress processor indicates said hardware classifier has been disabled.

5 - 8. (Canceled)

9. (Previously Amended) A network switch for enhancing execution of frame classification information comprising:

an ingress processor for parsing and recovering parameters from a frame and recovering the identity of said frame;

Serial No. 09/546,833**PATENT****Docket No. RAL920000042US1**

said ingress processor being further programmed to create a header for an intra-switch frame identifying said frame and a level of processing of said received frame;

an egress processor for receiving said intra-switch frame and for creating a frame for passing to one or more output ports, said egress processor being programmed to:

execute instructions which follow a starting address for completing processing of said frame;

forward said processed frame to an output port based on said processing of said frame; and

a hardware frame classifier, includes an address table which decodes frame header extension values and variable frame extension values which point to said egress processor starting address location, for determining from said intra-switch frame header said starting address of said instructions which are to be processed wherein the level of processing of said received frame includes code for identifying a beginning address of picocode instructions stored in said egress processor and data generated by said ingress processor, to be used as required by said pico instructions being executed.

10 - 24. (Canceled)

25. (Previously Presented) In a network switching system having an ingress processor for receiving incoming frames from a port of a network, and an egress processor having a port through which said frames are delivered, a method for enhancing processor speed by the egress processor comprising:

forming at said ingress processor a header for each frame destined for said egress processor said header having code for identifying a beginning address of picocode instructions stored in said egress processor; and

Serial No. 09/546,833**PATENT****Docket No. RAL920000042US1**

decoding said code in said header in a hardware frame classifier into a starting address in said picocode for said egress processor if said classifier is enabled otherwise executing processing of a frame beginning at a process execution level determined from a port configuration entry of the interface of the port said frame was received if a configuration bit of said egress processor indicates said hardware classifier has been disabled.

26. (Previously Presented) The method for enhancing processing according to claim 25 wherein said frame header includes control information for said egress processor which distinguish said frames as being multicast or unicast.

27. (Previously Amended) In a network switching system having an ingress processor for receiving incoming frames from a port of a network, and an egress processor having a port through which said frames are delivered, a method for enhancing processor speed by the egress processor comprising:

forming at said ingress processor a header for each frame destined for said egress processor having code for identifying a beginning address of picocode stored in said egress processor; and

decoding data in said header in a hardware frame classifier into a starting address in said picocode for said egress processor wherein decoding said code include indexing an address table in said hardware frame classifier; and

executing processing from a starting address space identified by said table of said hardware classifier if said hardware classifier is enabled, otherwise executing processing of a frame beginning at a process execution level determined from a port configuration entry of the interface of the port said frame was received if a configuration bit of said egress processor indicates said hardware classifier has been disabled.

Serial No. 09/546,833**PATENT****Docket No. RAL920000042US1**

28. (Previously Presented) The method for enhancing processing according to claim 25 wherein said egress processor creates multiple frames for multiple output ports when said frame header contains multicast data.

29. (Previously Amended) A network switch for enhancing execution of frame classification information comprising:

- an ingress processor for parsing and recovering parameters from a frame and recovering the identity of said frame;

- said ingress processor being further programmed to create a header for an intra-switch frame identifying a received frame and a level of processing of said received frame;

- an egress processor for receiving said intra-switch frame and for creating a frame for passing to one or more output ports, said egress processor being programmed to:

- a hardware frame classifier for determining from said intra-switch frame header a starting address of said instructions which are to be processed;

- executing processing of a frame beginning at a process execution level determined from a port configuration entry of the interface of a port said frame was received if a configuration bit of said egress processor indicates said hardware classifier has been disabled; and

- forward said processed frame to an output port based on said processing of said frame.

30. (Previously Presented) The network switch according to claim 29 wherein said hardware frame classifier includes an address table which decodes frame header extension values and variable frame extension values which point to said egress processor starting address location.

Serial No. 09/546,833**PATENT**
Docket No. RAL920000042US1

31. (Previously Amended) The network switch according to claim 29 wherein said frame header includes a field to identify said frame as being a multicast frame.

32. (Previously Presented) The network switch according to claim 29 wherein said frame header data is stored in fixed length fields which have a length determined by a length field in said header.

33. (Previously Presented) In a network switching system having an ingress processor for receiving incoming frames from a port of a network, and an egress processor having a port through which said frames are delivered, a method for enhancing processor speed comprising:

forming at said ingress processor a header for each frame destined for said egress processor said header having data identifying parameters computed by said ingress processor and code identifying a starting address of picocode instructions stored in said egress processor, and

decoding said code in said header in a hardware frame classifier into the starting address in said picocode for said egress processor if said classifier is enabled otherwise executing processing of a frame beginning at a process execution level determined from a port configuration entry of the interface of the port said frame was received if a configuration bit of said egress processor indicates said hardware classifier has been disabled.

34 - 35. (Canceled)

36. (Previously Amended) In a network switching system having an ingress processor for receiving incoming frames from a port of a network, and an egress processor having a port through which said frames are delivered, a method for enhancing processor speed by the egress processor comprising:

Serial No. 09/546,833**PATENT****Docket No. RAL920000042US1**

forming at said ingress processor a header for each frame destined for said egress processor said header having data for identifying a beginning of a processing sequence for said egress processor and control information for said egress processor which distinguish said frames as being multicast frame or unicast frame; and

decoding said data in said header in a hardware frame classifier into a starting address for said egress processor if said classifier is enabled otherwise executing processing of a frame beginning at a process execution level determined from a port configuration entry of the interface of the port said frame was received if a configuration bit of said egress processor indicates said hardware classifier has been disabled.

37. (Previously Presented) The method of claim 36 wherein the control information includes a single bit when set to a first state indicates the unicast frame and when set to a second state indicates the multicast frame.

38. (Previously Presented) In a network switching system having an ingress processor for receiving incoming frames from a port of a network, and an egress processor having a port through which said frames are delivered, a method for enhancing processor speed by the egress processor comprising:

forming at said ingress processor a header for each frame destined for said egress processor having data for identifying a beginning of a processing sequence for said egress processor;

decoding said data in said header in a hardware frame classifier into a starting address for said egress processor if said classifier is enabled otherwise executing processing of a frame beginning at a process execution level determined from a port configuration entry of the interface of the port said frame was received if

Serial No. 09/546,833

PATENT

Docket No. RAL920000042US1

a configuration bit of said egress processor indicates said hardware classifier has been disabled; and

creating multiple frames for multiple output ports when said frame header contains multicast data.